HIT 2 482-06

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Continuation Application under
37 CFR 1.53(b):

Prior Application:	T. WATANABE et al Serial No. 09/198,658 Filed: November 24, 1998
Group Art Unit:	2783
Examiner:	E. Coleman
For:	NEURAL NETWORK PROCESSING SYSTEM USING SEMICONDUCTOR MEMORIES

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above application as follows.

IN THE SPECIFICATION

Attached is a Substitute Specification, as filed in the original parent application, U.S. Serial No. 07/928,755, along with a "marked-up" copy of the original specification noting the changes made thereto. Applicants respectfully submit that no new matter has been added or presented in the Substitute Specification.

IN THE CLAIMS

Please cancel claim 1 and add new claim 25 as set forth below.

--25. A semiconductor integrated circuit device, comprising:

a memory array having a plurality of word lines, a plurality of bit lines, and a plurality of memory cells;

a processing circuit coupled to said memory array via a plurality of signal lines;

an input/output circuit coupled to one of the plurality of signal lines; and

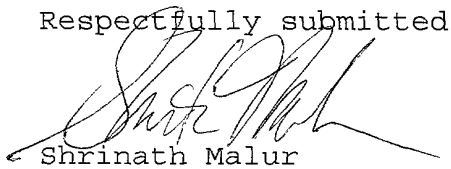
a switching circuit inserted between the plurality of signal lines and said input/output circuit.--

REMARKS

Claim 1 has been canceled. New claim 25 has been added. Accordingly, claim 25 is currently pending in the application.

Examination is respectfully requested.

Respectfully submitted,



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